PRA – 4. letnik

VAJA – PIC 16F877A

Dijak:	Razred: _
Člani skupine: 1.	Datum:
2.	
3.	

Oprema: Osebni računalnik, svetovni splet (internet), program Splan

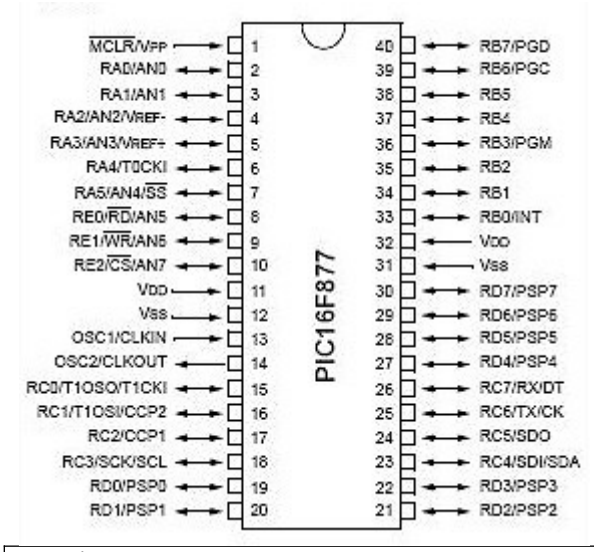
Naloga: Na svetovnem spletu najdite podatke o mikrokontrolerju PIC 16F877A, ter prenesite, ugotovite, izpišite in prevedite v slovenščino naslednje vsebine:

1. Vstavite pin diagram PIC-a 16F877A s podnožjem 40pin PDIP.
2. Vstavite sliko blok diagrama PIC16F877A.
3. Vstavite tabelo ukazov v zbirnem jeziku, ki jih pozna PIC 16F877A. Koliko ukazov pozna?
4. Opišite posamezne priključne sponke integriranega vezja v slovenščini (prevedite pinout description tabelo).
5. Izpiši in prevedi tabelo, kjer so podane električne lastnosti integriranega vezja in kaj pomeni Absolute Maximum Ratings?
6. Kakšno ločljivost ima A/D pretvornik, kam je priklopljen in koliko je največja in najmanjša dovoljena analogna napetost, ki jo smemo priključiti na vhod pretvornika? Kolikšen je minimalni čas zajemanja enega vzorca?
7. Odgovori na vprašanja: Kaj je oscilator? Zakaj je potreben? Kako in kam ga lahko priklopimo na naše integrirano vezje. Kakšne oscilatorje poznamo in kakšnega lahko priključimo na PIC16F877A?
8. Kolikor se da podrobno opiši CONFIGURATION WORD REGISTER, ki se nahaja na naslovu 2007h!
9. Iz podatkov ki si jih pridobil in s pomočjo programa za risanje električnih shem (Splan), nariši električno shemo: PIC16F877A + oscilator + napajanje (priključne sponke, transformator (220V / 12V), varovalka, usmerniški mostič, kondenzatorji, stabilizator nap.,...) + reset tipka (tipka,...) + na PORTC, izhod 5 priključi **12V** žarnico, ki bo svetila, ko bo izhod na logični **1 +** na PORTB, izhod 4 priključi **5V** rele + ter na PORTD, vhod 1 tipko, ki deluje kot vhodna spremenljivka in bo ob pritisku nanjo mikrokontroler na tem vhodu zaznal logično **0**.
10. Kaj je SPI in kaj bi priključil na te priključke?
11. S pomočjo svetovnega spleta najdi in vstavi 3. električne sheme, ki vsebujejo mikrokontroler PIC16F877A. Ob slikah dodaj opis kakšno vezje je to ter povezavo na stran kjer ste ga našli.
12. Za izbrano el. Shemo , s pomočjo SprintLayout4 programa nariši tiskano vezje.

*** Pred oddajo datoteke, jo preimenuj z imenom in priimkom, številko vaje ter razredom.
Primer:
Franc Bedanc – vaja1-R4A.doc

Poročilo oddajte v el. obiliki.

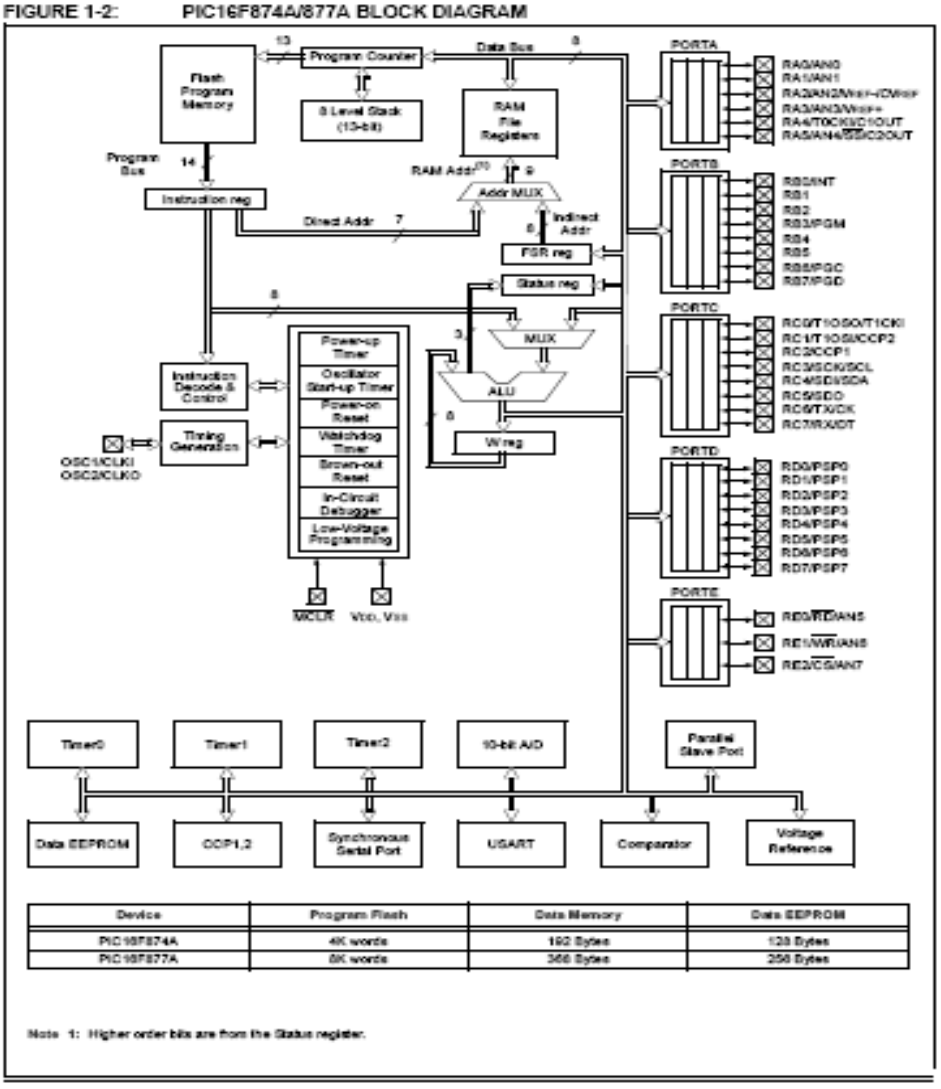
Rešitve:



OSC1/CLKI OSC1 CLKI	input
OSC2/CLKO OSC2 CLKO	.
MCLR/VPP MCLR VPP	Odlikujte se v () ().
RA0/AN0 RA0 AN0 RA1/AN1 RA1 AN1 RA2/AN2/VREF-/ CVREF RA2 AN2 VREFCVREF RA3/AN3/VREF+ RA3 AN3 VREF+ RA4/T0CKI/C1OUT RA4 T0CKI C1OUT RA5/AN4/SS/C2OUT RA5 AN4 SS C2OUT	PORTA I/ port Digital I/O. Analog input 0. Digital I/O. Analog input 1. Digital I/O. Analog input 2. A/D reference voltage (Low) input. Comparator VREF output. Digital I/O. Analog input 3. A/D reference voltage (High) input Digital I/O – Open-drain when configured as output. Timer0 external clock input. Comparator 1 output. Digital I/O. Analog input 4. SPI slave select input. Comparator 2 output

PIN1	MCLR-Master clear – aktivira reset napreve
PIN2	RA0/AN0 – dig. i/o; analogni imput 0
PIN3	RA1/AN1 - dig. i/o; analogni imput 1
PIN4	RA2/AN2 - dig. i/o; analogni imput 2
PIN5	RA3/AN3 - dig. i/o; analogni imput 3
PIN6	RA4/T0CKI/C1OUT – open drain ko je konfiguriran kot output
PIN7	RA5/AN4/SS/C2OUT – dig. i/o;
PIN8	RE0/RD/AN5 – bralni kontroler za paralelni slave port
PIN9	RE1/WR/AN6 – pisalni kontroler za paralelni slave port
PIN10	RE2/CS/AN7 – izbira vezja za paralelni slave port
PIN11	vdd
PIN12	vss
PIN13	OSC1/CLKI -
PIN14	OSC2/CLKO -
PIN15	RC0/T1OSO/T1CKI – digitalni i/o; časovni oscilator output
PIN16	Digitalni i/o; časovni oscilator imput
PIN17	Ujami input, primerjaj output
PIN18	Sinhronizirana serijska ura i/o
PIN19	Paralelni podatkovni slave port
PIN20	Paralelni podatkovni slave port
PIN21	Paralelni podatkovni slave port
PIN22	Paralelni podatkovni slave port
PIN23	RC4 je lahko tud SPI
PIN24	Input output port ali sinhroni serijski podatkovni port
PIN25	Input output port ali sinhrona ura
PIN26	Input/output pin ali sinhroni ali asinhroni prenosi
PIN27	i/o pin port ali paralelni slave port bit 4
PIN28	i/o pin port ali paralelni slave port bit 5
PIN29	i/o pin port ali paralelni slave port bit 6
PIN30	i/o pin port ali paralelni slave port bit 7
PIN31	vss
PIN32	vdd
PIN33	Digitalni i/o; zunanja prekinitev
PIN34	Digitalni i/o
PIN35	Digitalni i/o
PIN36	Digitalni i/o
PIN37	Digitalni i/o
PIN38	Digitalni i/o
PIN39	Debugger in ICSP programska ura
PIN40	Debugger in ICSP programski podatki

FIGURE 1-2: PIC16F874A/877A BLOCK DIAGRAM



PIC dobi na vhod RC3 signal iz komparatorja. Ta signal je pravokotni impulz amplitude 5V. PIC s pomočjo Timerja1, ki je 16 biten števec šteje prehode iz nič v ena. Te prehode šteje v intervalu 1s tako, da je rezultat že kar frekvenca. Zato ker je števec dolžine 16 bitov lahko izmerimo najvišjo frekvenco 2^n (n=16)=65536 Hz. Če presežemo to frekvenco pride do preliva in števec začne šteti od 0 naprej.

TABLE 15-2: PIC16F87XA INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add Literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND Literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to Address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR Literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from Interrupt	2	00	0000	0000	1001		
RETLW	k	Return with Literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from Literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR Literal with W	1	11	1010	kkkk	kkkk	Z	

Poznamo 35 ukazov.

17.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with respect to VSS (except VDD, $\overline{\text{MCLR}}$, and RA4) ..... -0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS ..... -0.3 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS **(Note 2)** ..... 0 to +14V
Voltage on RA4 with respect to Vss ..... 0 to +8.5V
Total power dissipation **(Note 1)** 1.0W
Maximum current out of VSS pin ..... 300 mA
Maximum current into VDD pin ..... 250 mA
Input clamp current, IIK (VI < 0 or VI > VDD) ..... ± 20 mA
Output clamp current, IOK (VO < 0 or VO > VDD) ..... ± 20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by PORTA, PORTB and PORTE (combined) **(Note 3)** ..... 200 mA
Maximum current sourced by PORTA, PORTB and PORTE (combined) **(Note 3)** ..... 200 mA
Maximum current sunk by PORTC and PORTD (combined) **(Note 3)** ..... 200 mA
Maximum current sourced by PORTC and PORTD (combined) **(Note 3)** ..... 200 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OI} \times I_{OL})$

2: Voltage spikes below VSS at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to VSS.

3: PORTD and PORTE are not implemented on PIC16F873A/876A devices.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AMR so tiste maksimalne zmogljivosti pri katerih lahko PIC še dela.

TABLE 17-14: A/D CONVERTER CHARACTERISTICS:PIC16F873A/874A/876A/877A (INDUSTRIAL)
PIC16LF873A/874A/876A/877A (INDUSTRIAL)

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
A01	NR	Resolution		—	—	10-bits	bit	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A03	EIL	Integral Linearity Error		—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A04	EDL	Differential Linearity Error		—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A06	EOFF	Offset Error		—	—	< ± 2	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A07	EGN	Gain Error		—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A10	—	Monotonicity		—	guaranteed(3)	—	—	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference Voltage (VREF+ – VREF-)		2.0	—	VDD + 0.3	V	
A21	VREF+	Reference Voltage High		AVDD – 2.5V		AVDD + 0.3V	V	
A22	VREF-	Reference Voltage Low		AVSS – 0.3V		VREF+ – 2.0V	V	
A25	VAIN	Analog Input Voltage		VSS – 0.3V	—	VREF + 0.3V	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source		—	—	2.5	kΩ	**(Note 4)**
A40	IAD	A/D Conversion Current (VDD)	PIC16F87XA	—	220	—	μA	Average current consumption when A/D is on **(Note 1)**
			PIC16LF87XA	—	90	—	μA	
A50	IREF	VREF Input Current **(Note 2)**		—	—	5	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see **Section 11.1 "A/D Acquisition Requirements"**.
				—	—	150	μA	During A/D conversion cycle

1. These parameters are characterized but not tested.

7.
Generator izmenične napetosti. V širšem pomenu vsak sistem, ki je zmožen mehaničnega ali električnega nihanja.; **harmonični ~** Telo, pri katerem je sila sorazmerna z odmikom iz ravnovesne lege in deluje proti raznovesni legi ali pri katerem je potencialna energija sorazmerna s kvadratom odmika.; **hertzov ~** Oscilator z anteno, ki oddaja elektromagnetno valovanje z valovno dolžino z velikostno stopnjo 1mH.

Oscilator je v bistvu pretvornik enosmerne električne moči v izmenično moč.nima odvisnosti vhod / izhod v elementarni funkciji.
Razlikujemo :

- Harmonični oscilatorji nihajo sinusno in je odstopanje izraženo v procentih.

Relaksacijski oscilatorji nihajo s pravokotnimi signali.Signal je sestavljen iz množice sinusnih signalov, ki se razlikujejo po amplitudi, frekvenci in fazi. Vsako obliko periodičnega signala lahko razstavimo na množico sinusnih signalov – Forierjeva analiza

14.2 Oscillator Configurations

14.2.1 OSCILLATOR TYPES

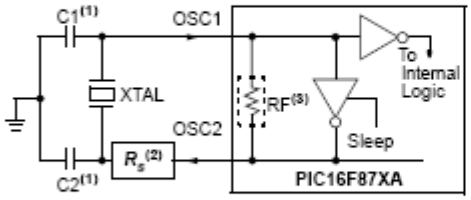
The PIC16F87XA can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low-Power Crystal
- XT Crystal/Resonator
- HS High-Speed Crystal/Resonator
- RC Resistor/Capacitor

14.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKI and OSC2/CLKO pins to establish oscillation (Figure 14-1). The PIC16F87XA oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKI pin (Figure 14-2).

FIGURE 14-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Table 14-1 and Table 14-2 for recommended values of C1 and C2.

2: A series resistor (R_S) may be required for AT strip cut crystals.

3: RF varies with the crystal chosen.

FIGURE 14-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

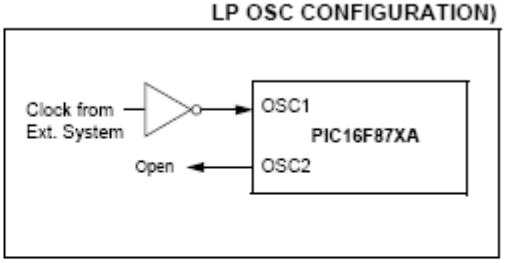


TABLE 14-1: CERAMIC RESONATORS

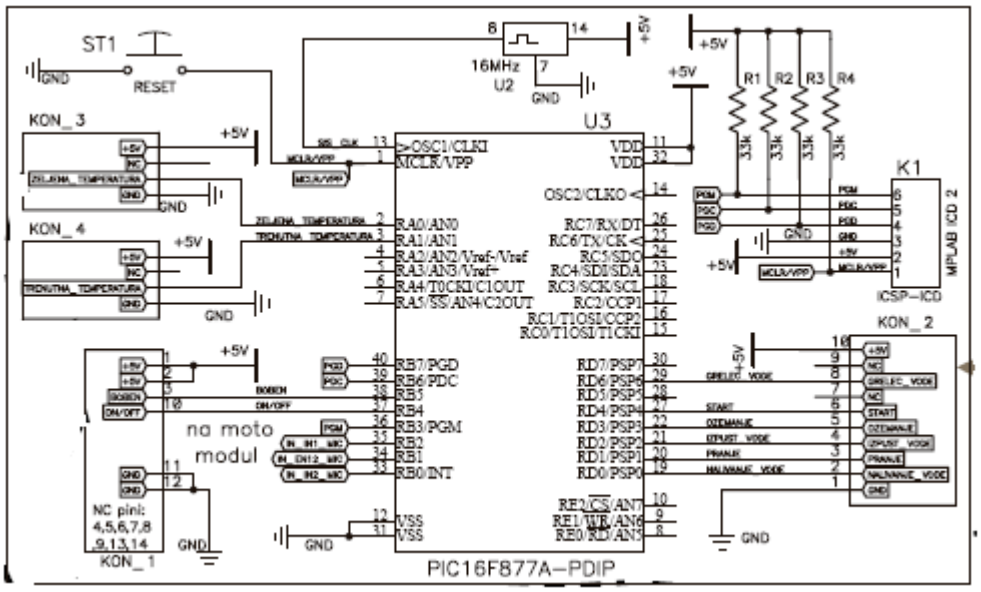
Ranges Tested:			
Mode	**Freq.**	**OSC1**	**OSC2**
XT	455 kHz 2.0 MHz 4.0 MHz	68-100 pF 15-68 pF 15-68 pF	68-100 pF 15-68 pF 15-68 pF
HS	8.0 MHz 16.0 MHz	10-68 pF 10-22 pF	10-68 pF 10-22 pF
These values are for design guidance only. See notes following Table 14-2.			
Resonators Used:			
2.0 MHz	Murata Erie CSA2.00MG	±0.5%	
4.0 MHz	Murata Erie CSA4.00MG	±0.5%	
8.0 MHz	Murata Erie CSA8.00MT	±0.5%	
16.0 MHz	Murata Erie CSA16.00MX	±0.5%	
All resonators used did not have built-in capacitors.			

8.

Configuration Bits:

bitov je a (a ‘0’),
ali pa neprogramirana(a ‘1’) za izbrano(naključno) komponentno konfiguracijo.
Vrednost za neporgramirano napravo je 3FFFh
Pomembno je, da je naslov 2007h za uporabnikovim spominsko prostornim, do katerega lahko dostopamo samo med programiranjem.

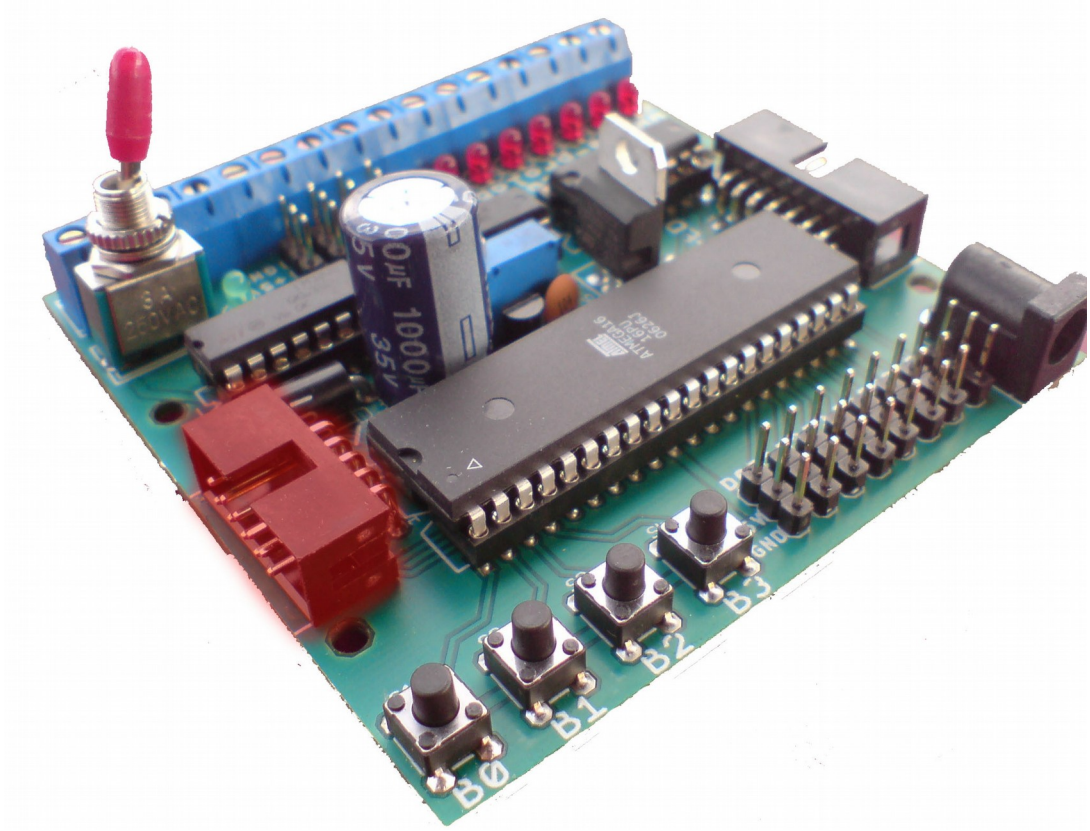
9.



Vezje, ki je uporabljeno pri pralnem stroju. Ima glavne potrebne elemente.

10.

Serial Peripheral Interface Bus



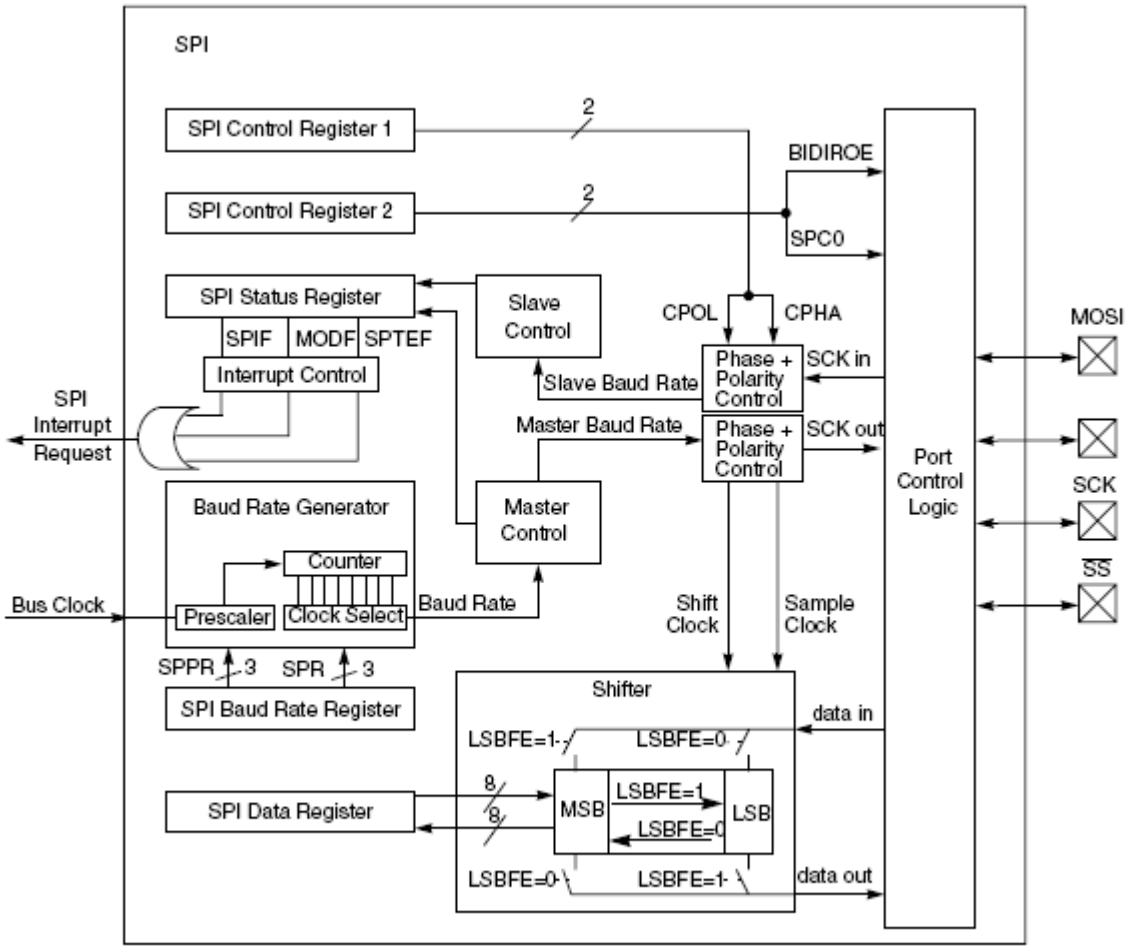
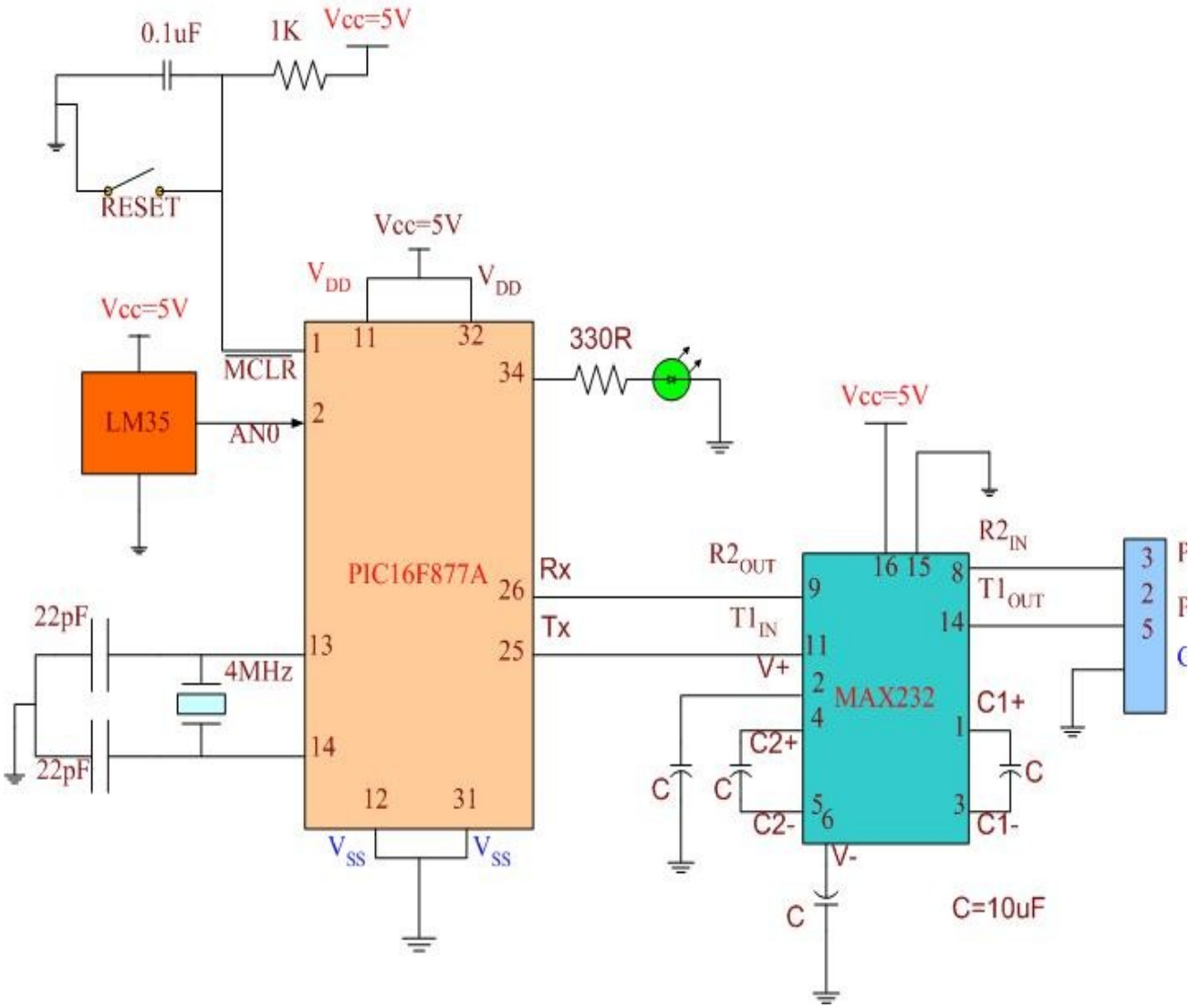
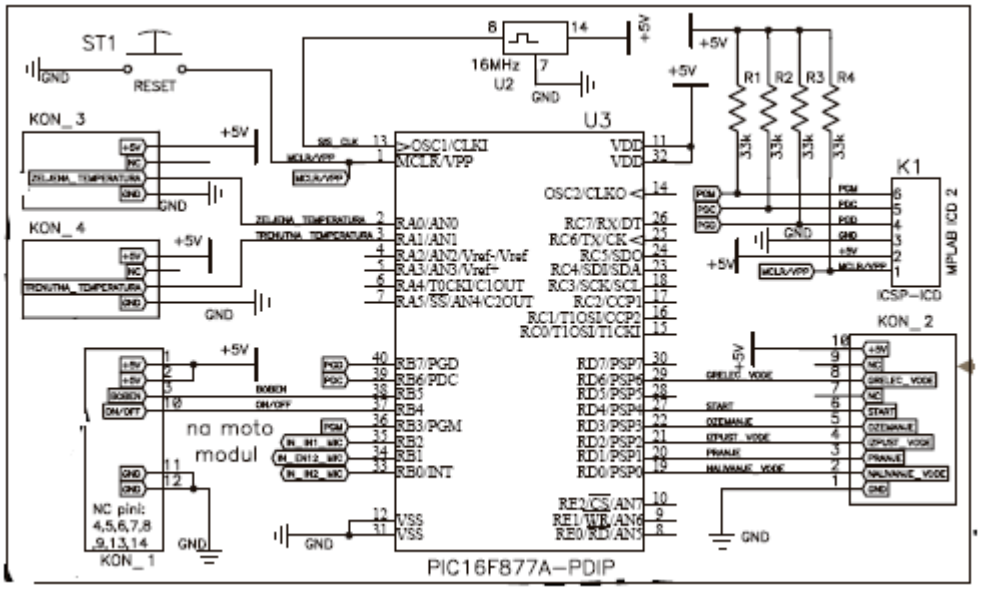


Figure 1-1. SPI Block Diagram

The SPI module allows a duplex, synchronous, serial communication between the MCU and peripheral devices.
Software can poll the SPI status flags or the SPI operation can be interrupt driven.

1





Shema prikazuje pralni stroj, ki sem ga našel v seminarski nalogi nekega študenta.